Muhammad M, Armstrong M, Elgendy M. Non-isolated DC-DC converter for high-step-up ratio applications. *In: 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*.
8-10 September 2015, Geneva, Switzerland: IEEE.

Non-isolated DC-DC Converter for High-Step-up Ratio Applications

Musbahu Muhammad, Matthew Armstrong, Mohammed Elgendy
School of Electrical & Electronic Engineering
Newcastle, United Kingdom
m.muhammad@ncl.ac.uk, matthew.armstrong@newcastle.ac.uk

Acknowledgements

The authors would like to acknowledge the Nigerian Petroleum Technology Development Fund (PTDF), and thank them for the invaluable PhD Scholarship Award for Musbahu Muhammad.

Keywords

High-step-up, non-isolated, coupled inductor, zero voltage switching (ZVS), Switched capacitor

Abstract

This paper presents a new Zero Voltage Switching (ZVS), non-isolated, boost converter for high voltage gain (greater than 10x) applications. A coupled inductor and two capacitors are used to enlarge the voltage gain of the power converter, without the need for extreme PWM duty ratio. Compared to similar power converter topologies presented in the literature, an important advantage of the proposed power electronic converter is the reduced voltage stress on the semiconductor devices. In this paper, the principle of operation of the circuit is described in full detail. Furthermore, experimental results, based on a 250W prototype power converter, are presented to validate the performance of the system. The proposed dc-dc power converter is particularly well suited to electrical vehicle and renewable energy applications, which typically have low input voltage and high output voltage requirements.

I. INTRODUCTION

Dc-dc boost converters are used to transfer power between low voltage sources to a higher dc bus. These converters are widely employed in applications such as uninterruptible power supplies UPS [1], Electric vehicles [2], photovoltaic systems [3], and high intensity discharge automotive headlamps [4]. In many modern applications, such as electric vehicle drives and grid connected PV systems, it is often necessary to achieve a stable steady state output voltage despite variation in the source voltage. Furthermore, the ratio of input voltage to output voltage can often be considerable. A conventional boost converter can be employed to increase the source voltage to the necessary voltage level required by the load. However, the conventional boost converter must operate at extreme duty ratios to achieve high voltage gains. This is an undesirable operating point, since the output diode sustains short pulse, high amplitude, current pulses which result in severe reverse recovery losses. In addition, as the output voltage increases so must the voltage rating of the semiconductor switching device and at high duty ratios the conduction losses of the semiconductor device can make a more significant impact to the performance of the system. Furthermore, as the duty cycle approaches unity, the converter may suffer poor dynamic response to system parameter changes and potential load variations [5].

To overcome these limitations of the conventional boost converter various high voltage gain, dc-dc converter topologies have been presented. One of the most widely chosen topologies is the isolated transformer coupled based converters [6, 7]. They are either current fed converters such as: current fed full and half bridges, dual boost and push full, or voltage fed converters such as: full bridge. The main drawback of this topology is volume increase of the magnetic component. Another approach for voltage gain improvement is switched capacitor/switched inductor converters [8, 9]. However, many switched capacitors cells are required to achieve high conversion ratio, which makes the circuit inherently complex. The major drawback of the switched inductor technique is the power device

voltage stress is equal to the output voltage; again high voltage rated devices potentially cause significant conduction losses. Alternatively, a common technique is to use a coupled inductor to enlarge the voltage gain in non-isolated dc/dc converter [10, 11]. Coupled inductor boost converters can provide high voltage gain without extreme duty cycle operation, with a relatively simple topology. Consequently, they can reduce the switch voltage stress and allow the use of low voltage rated, high performance, semiconductor devices. Miniaturization of the power converter circuit is possible if they operate at higher switching frequency. Furthermore, soft switching performance of coupled inductor converters will typically enhance the efficiency in high power applications [10, 11].However, the main drawbacks of coupled inductor converters typically include severe voltage spikes across the switch due to leakage energy of the leakage inductance and large input current ripple.

For this reason, this paper proposes a new boost dc-dc converter topology with the objective to achieve high voltage gain operation with a robust well regulated dc output voltage; whilst minimizing the semiconductor device stress typically observed in power converters of a similar type. To achieve this goal a high step up boost converter with coupled inductor and switched capacitors is adopted. Here, the two capacitors are charged in parallel by the coupled inductor and discharged in series to enlarge the voltage gain. Active clamping is employed to reduce the leakage energy of the leakage inductance and to realize zero voltage switching (ZVS) for all active devices. Importantly, this allows for low rated semiconductor devices to be used, which in turn helps to reduce conduction losses. Also, in the proposed circuit, the current falling rates of the diodes are alleviated by the leakage inductance of the coupled inductor. In the following, the operating principles of the proposed dc-dc converter are described in full detail. Experimental results from a 250 W prototype circuit are then presented to validate the advantageous performance and operation of the high voltage gain circuit.

II. PROPOSED CONVERTER AND ANALYSIS

A. Circuit Configuration and Description

The proposed converter topology is shown in Fig. 1(a): it consists of four key elements which include the dc source, coupled inductor primary side, coupled inductor secondary side, and a dc output. In the proposed circuit, the coupled inductor is denoted as L, and the primary and secondary windings of the coupled inductor are defined as L_a and L_b respectively. The primary winding L_a serves as a filter inductor (as in a conventional boost converter) and is coupled to the corresponding secondary windingL_b. The number of turns in the primary and secondary windings of the coupled inductor is represented by n_1 *and* n_2, and the coupling reference denoted by ‘’*’’. The main switch of the converter is denoted by S. An active clamp circuit is formed through clamping switch S_C and the clamp capacitor C_C. Furthermore, a voltage multiplier cell is present and consists of the coupling inductor secondary winding L_b, the clamp switch S_C, clamp capacitor C_C, regenerative diode D_r and the switched capacitor C_m. D_O and C_O are the output diode and filter capacitor; R_O denotes the output resistive load.

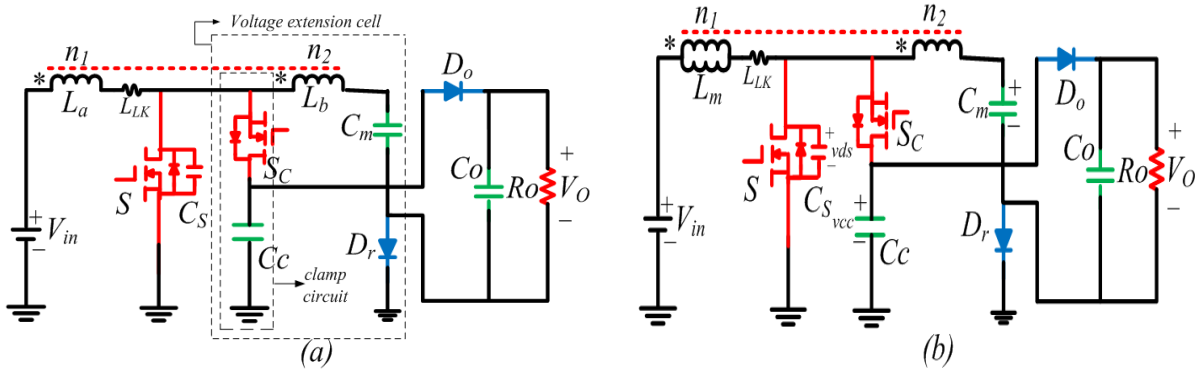


Fig. 1: Proposed non-isolated high step up boost converter
(a) Converter circuit diagram (b) equivalent circuit

Fig. 1(b) shows the equivalent circuit of the proposed high step-up boost converter. The coupled inductor can be modeled as an ideal transformer with defined turns ratio, *N*. Considering an ideal transformer, the primary winding is in parallel with magnetizing inductor L_m and then in series with a leakage inductance L_{Lk} [10, 11]. The turns ratio and coupling coefficient, *k,* of the ideal transformer are expressed as

$$N = \frac{n_2}{n_1} \tag{1}$$

$$k = \frac{L_m}{L_{Lk} + L_m} \tag{2}$$

C_S denotes the parallel capacitor of the main switch S (see Fig. 1b), including the parasitic capacitors of the main switch and the possible added parallel capacitor. V_{in} and V_O are the input and output voltages of the converter respectively.

B. Proposed Converter Operational Analysis

The proposed converter is designed to operate in continuous conduction mode (CCM). During steady state operation, the duty cycle D is higher than 0.5. The gate signal of the clamp switch S_C, is complimentary to that of main switch S (see Fig. 1). The steady state waveform of the proposed converter is shown in Fig. 2. There are six stages in one switching cycle. For completeness, the equivalent circuit corresponding to each operational stage is shown in Fig. 3.

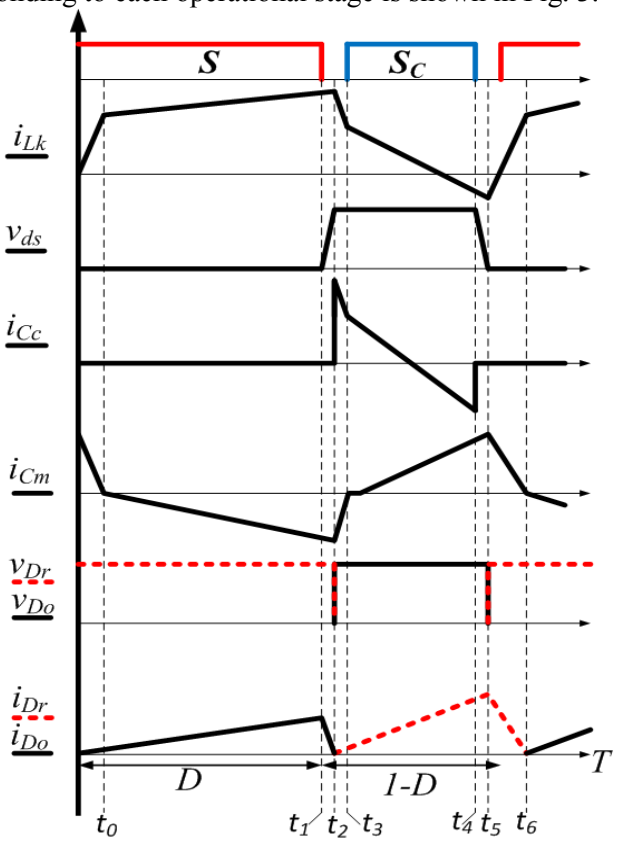


Fig. 2: Theoretical steady state waveform of high voltage gain dc-dc converter

Stage 1 $[t_0 - t_1]$: Before t_0 the main switch S_l is conducting, whilst the clamp switch S_C, is turned off. Magnetizing inductance L_m is charged linearly by the input voltage source V_{in}. The regenerative diode D_r is reversed biased and the output diode D_O is forward biased. During this time the clamp capacitor, the multiplier capacitor and the coupled inductor secondary winding are in series to enlarge the voltage gain. The magnetizing and leakage currents are

$$i_{Lm}(\mathrm{t}) = I_{\mathrm{Lm}}(t_0) + \frac{V_{in}}{L_m}(t - t_0) \tag{3}$$

$$i_{Lk}(\mathrm{t}) = i_{Lk}(t_0) + \frac{V_{in} - (V_{out} - V_{Cm} - V_{CC})/N}{L_{Lk}}(t - t_0) \tag{4}$$

Stage 2 $[t_1 - t_2]$: At time t_1 the main switch turns off, the parallel capacitor C_S is charge by the leakage inductor current i_{Lk}. The parallel capacitor begins to resonate with leakage inductance L_{LK}. Due to the fact that i_{Lk} is relatively large and C_S is small, the drain source voltage v_{ds} of the main switch rises with constant slope from zero. The turn off losses of the main switch S is reduced because of C_S. v_{ds} is given by

$$v_{dS} \approx \frac{I_{LK}(t_1)}{C_s}(t - t_1) \tag{5}$$

Stage 3 $[t_2 - t_3]$: At t_2, the voltage across the main switch rises slightly higher than the clamp capacitor voltage which makes the antiparallel diode of the clamp switch to conduct. The gate signal of the clamp switch S_C can be applied to implement ZVS turn on whilst it antiparallel diode is conducting. v_{ds} is clamped to v_{CC} by the antiparallel diode of the clamp switch S_C. The current flow through the clamp capacitor and the leakage inductance current decreases at approximately linear rate given by

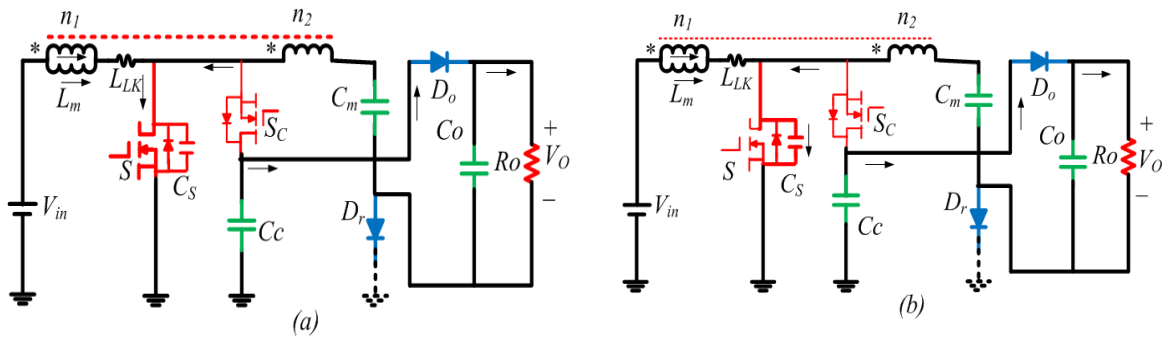
$$i_{LK}(\mathrm{t}) - i_{LK}(t_2) - \frac{V_{CC}}{L_{LK}}(t - t_2) \tag{6}$$

Stage 4 $[t_3 - t_4]$: the clamp switch S_C turns on with ZVS at time t_3 . The output diode becomes reversed biased and the diode D_r is forward biased. The energy stored in the magnetizing inductor L_m and leakage inductor L_{LK} begins to transfer to clamp capacitor C_C. The clamp capacitor C_C, the switched capacitors C_m are now charged in parallel by the input voltage source. A resonance is formed between the capacitors and leakage inductance.

Stage 5 $[t_4 - t_5]$: the clamp switch S_C is turned off at t_4. The clamp capacitor, switched capacitor and leakage inductance stop resonating. A new resonance is formed by the leakage inductance and parallel capacitor of the main switch. The drain source voltage of main switch decreases with constant slope and that of clamp switch increases linearly from zero. C_S reduces the turn off losses of the main switch.

$$v_{dS} \approx V_{CC} + \frac{I_{LK}(t_5)}{C_s}(t - t_4) \tag{7}$$

Stage 6 $[t_5 - t_6]$: at t_5 the voltage across the parallel capacitor reduces to zero. Then the antiparallel diode of the main switch begins to conduct. The gate signal of the main switch can be applied at this instant to implement ZVS turn on. After this a new switching cycle begins in the same fashion.



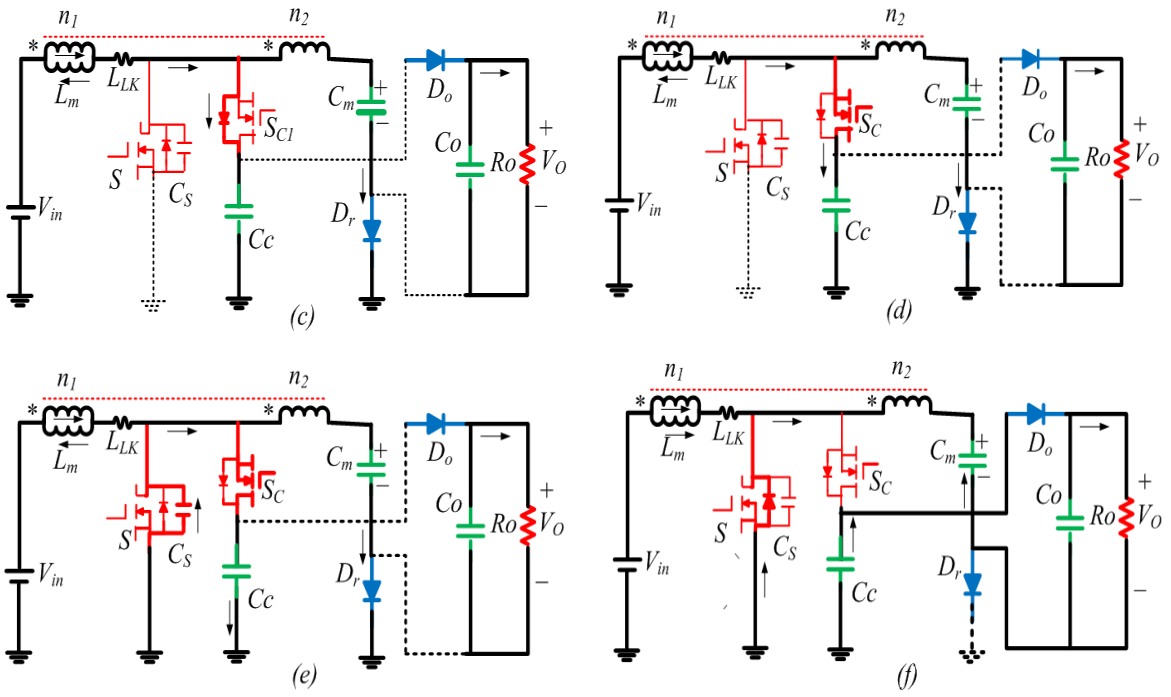


Fig. 3: Operational stages equivalent circuits
(a) Stage 1 $[t_0 - t_1]$, (b) Stage 2 $[t_1 - t_2]$, (c) Stage 3 $[t_2 - t_3]$, (d) Stage 4 $[t_3 - t_4]$, (e) Stage 5 $[t_4 - t_5]$, (f) Stage 6 $[t_5 - t_6]$.

III. STEADY STATE CONVERTER ANALYSIS

A. Voltage Gain

Under ideal conditions, the coupled inductors are assumed to be well coupled and the leakage inductance is ignored. The power switch is ideal with zero conduction voltage drops. The voltage on the clamp capacitor, output capacitor and switched capacitor are considered to be constant. The voltage of the parallel capacitors is zero; when the main power switch is turned on, the magnetizing inductor is charged by the input voltage, and the voltage across the magnetizing inductor can be defined as

$$V_{Lm} = V_{\text{in}} \tag{8}$$

The voltage across the secondary winding of the coupled inductor

$$V_{Lb} = NV_{Lm} \tag{9}$$

During the same instant, the diode D_r is off and the output diode D_O is on, the clamp capacitor and switched capacitor discharge in series, the power is transferred from the input to the output; the output voltage can be described by

$$V_o = V_{Cm} + V_{CC} + NV_{\text{in}} \tag{10}$$

the voltage on the clamp capacitor is given by

$$V_{Cc} = V_{ds} = V_{dsc} = \frac{V_{in}}{(1-D)} \tag{11}$$

Where V_{dsc} is the voltage across the clamp switch. At the instant when the main switch S turns off, the clamp switch turns on after some time delay and the clamp and switched capacitors are charged in parallel. The voltage across the switched capacitor is denoted as:

$$V_{Cm} = N(V_{CC} - V_{in}) + V_{CC} \tag{12}$$

From (10), (11) and (12) the ideal voltage gain is given by

$$M_{ideal} = \frac{V_o}{V_{in}} = \frac{N+2}{(1-D)} \tag{13}$$

It is evident from (13), that the proposed converter has the potential for high conversion ratio; through proper turns ratio design of the coupled inductor, there is a means of enlarging the voltage gain without resorting to extreme PWM duty ratio operation.

In practice, it is impossible to achieve 100% coupling between the coupled inductor windings. From the steady state analysis in the previous section, the leakage inductance is responsible for realizing the ZVS for both main and clamp switches. Once the leakage inductance is considered the voltage gain is given by

$$M = \frac{V_o}{V_{in}} = \frac{N+2}{(1-D)} \cdot \frac{1}{1 + 2 \cdot Q \cdot N^2/D^2 + 2 \cdot Q \cdot N^2/(1-D)^2} \tag{14}$$

Where $Q = L_{LK} f_S / R_o$ and $f_S$is the switching frequency and R_o is the load resistor. According to (14), it can be concluded that the voltage gain is related to the switching frequency $f_{s,}$ load resistor R_o, and the leakage inductance L_{Lk}, in addition to the turns ratio of the coupled inductors and the duty cycle D. The characteristic curve relating the voltage gain to the duty cycle for a given leakage inductance is shown in Fig. 4. With turns ratio N equal to 2, it is evident that the leakage inductance degrades the voltage conversion ratio; hence confirming the need for good quality inductor design.

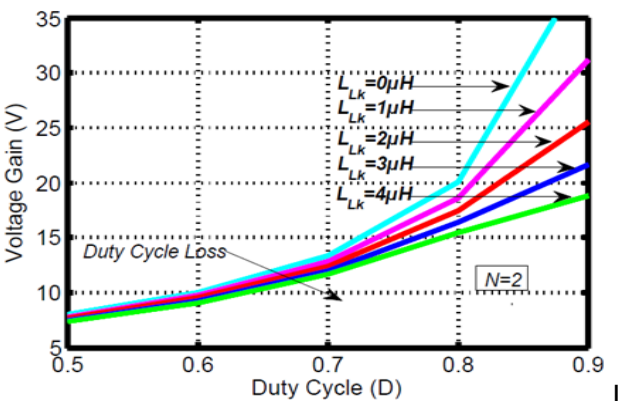


Fig. 4: Effect of leakage inductance on power converter voltage gain

B. Voltage and Current Stress Analysis

To simplify the voltage and current stress analysis on the converter devices, the voltage ripple on the capacitors may be ignored. The voltage stress on main and clamp switches are given by

$$V_{ds} = V_{dsc} = \frac{V_{in}}{(1-D)} \tag{15}$$

The voltage stress of the main and clamp switches in terms of output voltage and coupled inductor turns ratio can be expressed as

$$V_{ds} = V_{dsc} = \frac{V_{out}}{N+2} \tag{16}$$

Clearly, the voltage stress of the main and clamp switches reduce as the turns ratio increases. Note, the switch voltage stress is not dependent on the duty cycle and the input voltage. Provided the output voltage and the turns ratio remains fixed, the maximum voltage across the switch will remain constant.

The voltage stress of the output diode D_O and the regenerative diode D_r is the same and increases as the turns ratio of the coupled inductor increases, however, it is always lower than the output voltage and is expressed as:

$$V_{DO} = V_{Dr} = V_O - V_{CC} = \frac{(N+1)V_{in}}{(1-D)} \tag{17}$$

The RMS current of main and clamp switch is given by

$$I_{RMS-S} = \frac{(N+2)I_{out}}{(1-D)}\sqrt{D + \frac{2N(1-D)}{(N+2)} + \frac{4N^2(1-D)^2}{3D(N+2)^2}} \tag{18}$$

$$I_{RMS-SC} = I_{in}\sqrt{\frac{4N^2(1-D)}{3(N+2)^2D^2} - \frac{(2N+D-ND)(N-1)(1-D)}{D(N+2)^2}} \tag{19}$$

C. Performance Comparison

In order to better appreciate the advantages of the proposed topology, a performance comparison is made between coupled inductor boost converter with buck-boost active clamp [10], active clamp coupled inductor converter with extended voltage doubler cell [11], and the converter proposed here. As shown in Table I, the proposed converter can realize the same or higher voltage conversion ratio with a lower turns ratio of the coupled inductor, when compared to the other two topologies. Lower turns ratio reduces the copper loss. With regards to the output diode voltage stress, the output diode voltage stress in the buck-boost converter [10] is higher than the output voltage, and the rectifier reverse recovery losses will be significant. In case of the power converter in [11], the voltage stress of the diode is the same as the output voltage. However, in the proposed topology the diode voltage stress is always less than the output voltage, and this has the advantage of reducing the diode reverse recovery losses in high power applications. It is worth mentioning that the proposed converter does not require any start up circuitry. However, a start-up process is recommended in [11] to limit the inrush current.

Table I: Performance comparison between Converter in [10], Converter in [11] and Proposed Converter.

Topology	Converter In [10]	Converter In [11]	Proposed Converter
Active Switches	2	2	2
Diodes	1	2	2
Voltage gain	$\frac{(1+ND)}{(1-D)}$	$\frac{(1+N)}{(1-D)}$	$\frac{(2+N)}{(1-D)}$
Voltage stress of main switch	$\frac{V_{out}}{(1+ND)}$	$\frac{V_{out}}{1+N}$	$\frac{V_{out}}{2+N}$
Voltage stress of output rectifier	$\frac{(1+N)V_{out}}{(1+ND)}$	V_{out}	$\frac{(1+N)V_{out}}{(2+N)}$
Soft switching	ZVS	ZVS	ZVS
Switching Losses	Low	Low	Low

IV. DESIGN CONSIDERATION

A. Turns Ratio Selection

The key design step is to choose the coupled inductor turns ratio from (20), because it determines the duty cycle, power device current and voltage requirements

$$N = \frac{V_O(1-D)}{V_{in}} - 2 \tag{20}$$

B. Magnetizing Inductor Design

The peak value of the magnetizing inductor current is given by (21), from which the magnetizing inductor can be designed by setting an acceptable current ripple.

$$\Delta I_{Lm} = \frac{V_{in\_min} \cdot D}{L_m \cdot f_S} \tag{21}$$

C. Leakage Inductor Design

The leakage inductance is derived from (14) and expressed as

$$L_{LK} \leq \frac{R_0 D^2 (1-D)[(N+1) - M(1-D)]}{2N^2 M f_s (1 - 2D + 2D^2)} \tag{22}$$

D. Clamp and Switched Capacitors Selection

They key design parameter is to suppress the ripple voltage on both the clamp and the switched capacitor to an acceptable range. A reasonable compromise for the clamp capacitor value is to select the closest value so that one half of the resonant period exceeds the maximum turn off time of the main switch [4]. This is given by

$$C_C \geq \frac{(1-D)^2}{\pi^2 L_{LK} {f_s}^2} \tag{23}$$

The switched capacitor serves as a voltage source in the converter. The relationship between the output current and the voltage ripple in the switched capacitor can be derived as

$$C_m = \frac{I_{out}}{\Delta v_C f_S} \tag{24}$$

Where Δv_C is the voltage ripple on the switched- capacitor.

E. Power Device Selection

The power devices can be selected from (19) by considering an acceptable voltage and current margins

V. EXPERIMENTAL RESULTS

To verify the performance of the converter a 250 W prototype was implemented in the laboratory. The specifications are as follows:

1. Dc input voltage V_{in}: 20 V
2. Dc output voltage V_o: 190 V
3. Output power P_{out}: 250 W
4. Switching frequency f_s: 50 KHz
5. Mosfet switch S and S_c: FDP047AN08A0
6. Diodes D_o and D_r:MBR40250 G
7. Coupled Inductor: Kool mu core, N=1:1.8, L_m=*84* µH, L_{Lk}: 1.5 µH
8. Capacitors: C_C:4.7 µF, C_m:10 µF, C_o:220µF

Fig. 5 shows the experimental waveform of the proposed converter at full load with 20 V input voltage. The complimentary gate signals of the main, clamp switches and inductor current are shown in Fig. 5a. The duty ratio of the main switches is 0.67, which demonstrates that a modest duty cycle can be utilized. The clamp circuit performance is shown in Fig. 5b; the drain source voltage of the main and clamp switches are clamped at appropriately 60 V. It can be seen that when the main switch turns-off, the clamping capacitor begins to charge. The ZVS of the main and clamp switch are shown in Fig 5c,; the waveforms confirm the converter analysis described in Section III. The current and

voltage waveforms of the output and regenerative diodes are shown in Fig 5d. This shows the ZCS turn off and the current falling rate of the diodes, hence minimal reverse recovery loss. It can also be observed that the voltage stress of the diodes is less than the output voltage of the converter, a key operational advantage of the proposed circuit. A maximum efficiency of 94.8% is recorded at 50 W and the lowest efficiency is 90% at 250 W. Note, this is only a laboratory prototype; improved coupling between the windings would have improved the efficiency performance of the circuit and the results demonstrate the importance of optimizing the characteristics of this component.

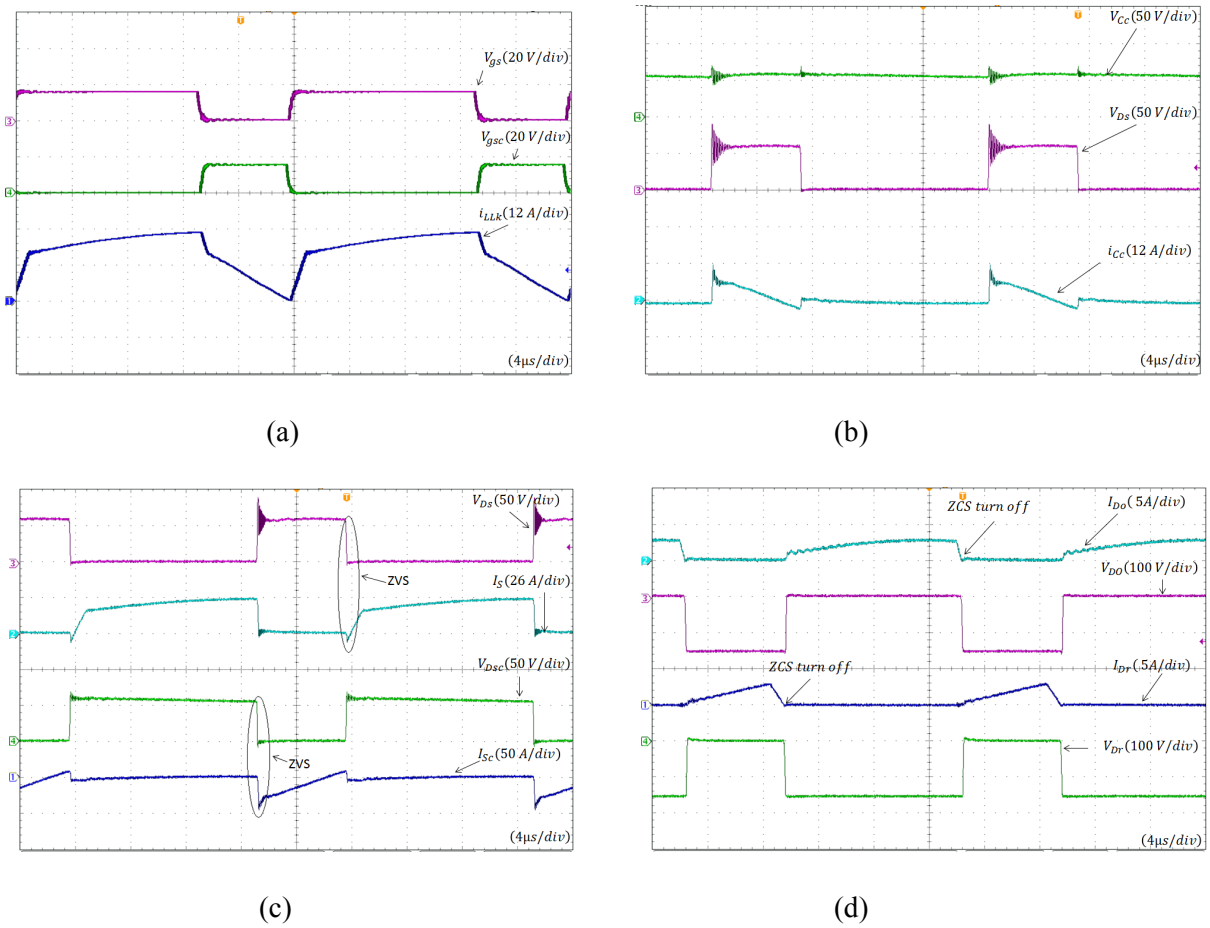


Fig. 5: Experimental waveforms

VI. CONCLUSION

This paper presents a new single phase, high gain, boost converter with coupled inductor and switched capacitor. This paper presents a full analysis of the circuit's principle of operation. Experimental results presented from a 250 W prototype have demonstrated the effectiveness and efficiency of the proposed topology as a high gain step-up converter. In high step-up applications extreme duty cycle operation, switching losses, high switch voltage stresses and severe reverse recovery diode losses are the main limitations of conventional boost converter topologies. Therefore, it can be concluded that the key advantages of the proposed converter are:

1. The voltage gain is easily enlarged by selecting the turns ratio of the coupled inductor.
2. Semiconductor switch voltage stress is reduced; hence lower voltage rated devices can potentially be adopted to reduce conduction losses.
3. ZVS soft switching performance is readily achieved for the main and clamp switches, further reducing losses in the circuit.

4. The current falling rate of the output diode is alleviated by the leakage inductance of the coupled inductor. The output and regenerative diodes turn off softly, minimizing reverse recovery loss.
5. The leakage energy of the coupled inductor is recycled to the output.

REFERENCES

[1] Haimin, T., J.L. Duarte, and M.A.M. Hendrix, Line-Interactive UPS Using a Fuel Cell as the Primary Source. Industrial Electronics, IEEE Transactions on, 2008. **55**(8): p. 3012-3021.

[2] James P, Forsyth A, Calderon-Lopez G, Pickert V. DC-DC converter for hybrid and all electric vehicles. In: The 24th International Battery, Hybrid and Fuel Cell Electric Vehicle Symposium and Exhibition (EVS 2009). 2009, Stavanger, Norway.

[3] Kuo-Ching, T., H. Chi-Chih, and S. Wei-Yuan, A High Step-Up Converter With a Voltage Multiplier Module for a Photovoltaic System. Power Electronics, IEEE Transactions on, 2013. **28**(6): p. 3047-3057.

[4] Qun, Z. and F.C. Lee, High-efficiency, high step-up DC-DC converters. Power Electronics, IEEE Transactions on, 2003. **18**(1): p. 65-73.

[5] W. Li, and X. He, "Review of Nonisolated High-Step-Up DC/DC Converters in Photovoltaic Grid-Connected Applications," IEEE Trans. Ind. Electron., vol **58** no.4, pp. 1239-1250,Apr, 2011.

[6] J. M. Kwon, E. H. Kim, B. H. Kwon, and K. H. Nam, "High-efficiency fuel cell power conditioning system with input current ripple reduction,"

IEEE Trans. Ind. Electron, vol. 56, no. 3, pp. 826–834, Mar. 2009.

[7] J. M. Kwon and B. H. Kwon, "High step-up active-clamp converter with input-current doubler and output-voltage doubler for fuel cell power systems," IEEE Trans. Power Electron, vol. 24, no. 1, pp. 108–115, Jan, 2009.

[8] F. Zhang, L. Du, F.Z. Peng and Z. Qian, "A New Design Method for High-Power High-Efficiency Switched-Capacitor DC-DC Converters ." IEEE Trans. Power Electron, vol. **23**, no. 2. pp. 832-840, Mar,2008.

[9] B. Axelrod, Y. Berkovich, and A. Ioinovici,"Switched- Capacitor/Switched-Inductor Structures for getting Transformerless Hybrid DC-DC PWM Converters." IEEE Trans. Circuit and Sys, vol **55**, no 2, pp. 687-696, Mar,2008.

[10] T. Wu, Y. lai, J.C. Hung and Y. Chen, "Boost Converter With Coupled Inductors and Buck-Boost Type of Active Clamp." IEEE Trans. Ind. Electrons,vol **55**, no. 1. pp. 154-162, Jan,2008.

[11] Y. Zhao, W. Li and X. He, "Single-Phase Improved Active Clamp Coupled-Inductor-Based Converter With Extended Voltage Doubler Cell." IEEE Trans. Power Electron, vol **27**, no 6, pp. 2869-2878, Jun,2012.

[12] Wuhua, L., et al., Single-Stage Single-Phase High-Step-Up ZVT Boost Converter for Fuel-Cell Microgrid System. Power Electronics, IEEE Transactions on, 2010. **25**(12): p. 3057-3065.

[13] Giaouris D, Stergiopoulos F, Ziogou C, Ipsakis D, Banerjee S, Zahawi B, Pickert V, Voutetakis S, Papadopoulou S. Nonlinear Stability Analysis and a New Design Methodology for a PEM Fuel Cell Fed DC-DC Boost Converter. International Journal of Hydrogen Energy 2012, **37**(23), 18205-18215.

[14] Yi Z, Li W, Yan D, He X, Lambert S, Pickert V. High step-up boost converter with coupled inductor and switched capacitor. In: 5th IET International Conference on Power Electronics, Machines and Drives (PEMD). 2010, Brighton, UK: IEEE.

[15] Li W, Li W, He X, Lambert S, Pickert V. Performance analysis of ZVT interleaved high step-up converter with built-in transformer. In: 5th IET International Conference on Power Electronics, Machines and Drives (PEMD). 2010, Brighton, UK: IEEE.